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1 **Implementation of 13 kbps QCELP vocoder ASIC**
Kyung-Jin Byun; Minsoo Hahn; Kyung-Su Kim;
ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on , 23-25 A 1999
Pages:258 - 261

[Abstract] [PDF Full-Text (340 KB)] **IEEE CNF**

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Nagamatsu, M.; Tago, H.; Mijamori, T.; Kamata, M.; Murakami, H.; Ootaguro, Goto, H.; Utsumi, T.; Teruyama, T.; Mabuchi, K.; Kawasumi, A.; Malik, K.;
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[Abstract] [PDF Full-Text (688 KB)] **IEEE CNF**

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3 **A 1.2 W 66 MHz superscalar RISC microprocessor for set-tops, video games, and PDAs**
Dac Pham; Kahle, J.; Ogden, D.; Putrino, M.; Tai Ngo; Hoover, K.; Cang Tran; Sweet, M.; Hung Hua; Quan Nguyen; Mallick, S.; Eisen, L.; Loper, A.; Chitturi Lyon, T.; Ho, B.; Patel, R.; Cheesebrough, E.; Kuttanna, B.; Piejko, A.;
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Yamamoto, T.; Gotoh, S.-I.; Takahashi, T.; Irie, K.; Ohshima, K.; Mimura, N.;
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1 **Vector instruction set support for conditional operations**
Smith, J.E.; Faanes, G.; Sugumar, R.;
Computer Architecture, 2000. Proceedings of the 27th International Symposiu on , 10-14 June 2000
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1 **Sequential logic optimization for low power using input-disabling precomputation architectures**
Monteiro, J.; Devadas, S.; Ghosh, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 3 , March 1998
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